USER MANUAL AND SPECIFICATIONS

MT1105

Baseband Transmitter Adapter Module

The MT1105 is an Baseband Transmitter adapter module designed to work in conjunction with your NI FlexRIO™ FPGA module. The MT1105 features the following connectors and chips:

- 8-channel, 250 MS/s (1.0GS/s after interpolation) digital-to-analog converter (DAC) with 16-bit accuracy
- Timing chip with clocking options from the backplane and the front panel
- The following front panel connectors:
  - CLK IN
  - AO 0
  - AO 1
  - AO 2
  - AO 3
  - AO 4
  - AO 5
  - AO 6
  - AO 7
  - DIO

This document contains signal information and lists the specifications of the MT1105, which is composed of the NI FlexRIO FPGA module and the MT1105. This document also contains tutorial sections that demonstrate how to acquire data using a LabVIEW FPGA Example VI and how to create and run your own LabVIEW project with the MT1105.

Note MT1105 refers to the combination of your MT1105 adapter module and your NI FlexRIO FPGA module. MT1105 refers to your MT1105 adapter module only.

Note The MT1105 is only compatible with the NI PXIe-796*x*R FPGA modules.

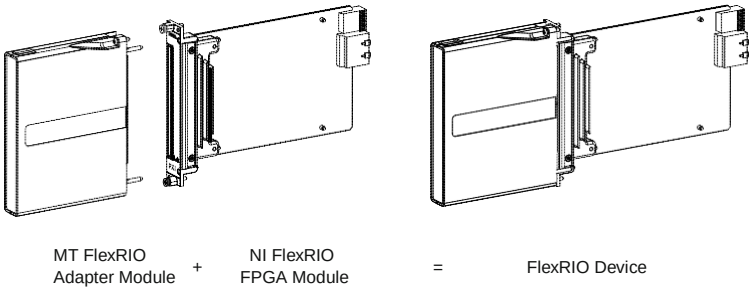
Note Before configuring your MT1105, you must install the appropriate software and hardware. Refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications* for installation instructions

Note For EMC compliance, operate this device according to the documentation.

Mush Technologies

The following figure shows an example of a properly connected FlexRIO device.

Figure 1. FlexRIO Device



Related Information

MT1105 Specifications on page 17

Contents

Electromagnetic Compatibility Guidelines

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC) stated in the product specifications. These requirements and limits are designed to provide reasonable protection against harmful interference when the product is operated in the intended operational electromagnetic environment.

This product is intended for use in industrial locations. However, harmful interference may occur in some installations, when the product is connected to a peripheral device or test object, or if the product is used in residential or commercial areas. To minimize interference with radio and television reception and prevent unacceptable performance degradation, install and use this product in strict accordance with the instructions in the product documentation.

Furthermore, any modifications to the product not expressly approved by National Instruments could void your authority to operate it under your local regulatory rules.

Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

Caution To ensure the specified EMC performance, the length of all I/O cables must be no longer than 3 m (10 ft).

Caution To ensure the specified EMC performance, you must install PXI EMC Filler Panels (National Instruments part number 778700-1) in adjacent chassis slots.

Related Information

Installing PXI EMC Filler Panels on page 23

Connecting Cables

1. Use any shielded 50Ω SMB cable to connect signals to the connectors on the front panel of your device.

Related Information

MT1105 Specifications on page 17

Key Features

The MT1105 includes the following key features:

RF frequency range..... DC to 120 MHz (DC coupled Option 01)
400 kHz to 120 MHz (AC coupled Option 02)

Instantaneous bandwidth.....120 MHz

DAC.....16-bit 8 channel at 250 MS/s, interpolated to 1 GS/s

Configuration

You can configure the MT1105 as follows:

- Instantaneous bandwidth up to 120 MHz
- 8 SE transmitter channel, 16-bit, 1GS/s (4× interpolation)

Front Panel and Connector Pinouts

Table 2 shows the front panel connector and signal descriptions for the MT1105.

Caution To avoid permanent damage to the MT1105, disconnect all signals connected to the MT1105 before powering down the module, and connect signals only after the adapter module has been powered on by the NI FlexRIO FPGA module

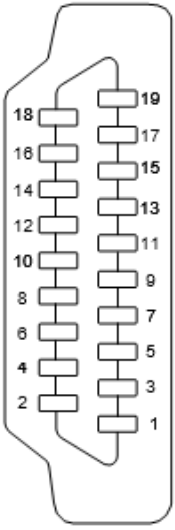
Caution Connections that exceed any of the maximum ratings of any connector on the MT1105 can damage the device and the chassis. NI is not liable for any damage resulting from such connections.

Related Information
MT1105 Specifications on page 15

Device Front Panel	Connector	Signal Description
	CLK IN	Reference Clock input, 50 Ω single-ended, +20 dBm maximum
	AO 0	Analog Output Channel 0, single-ended analog output channel
	AO 1	Analog Output Channel 1, single-ended analog output channel
	AO 2	Analog Output Channel 2, single-ended analog output channel
	AO 3	Analog Output Channel 3, single-ended analog output channel
	AO 4	Analog Output Channel 4, single-ended analog output channel
	AO 5	Analog Output Channel 5,single-ended analog output channel
	AO 6	Analog Output Channel 6, single-ended analog output channel
	AO 7	Analog Output Channel 7, single-ended analog output channel
	DIO	Refer to Table 3 for the signal list and descriptions.

DIO Connector

Table 3. MT1105 DIO Connector Pin Assignments

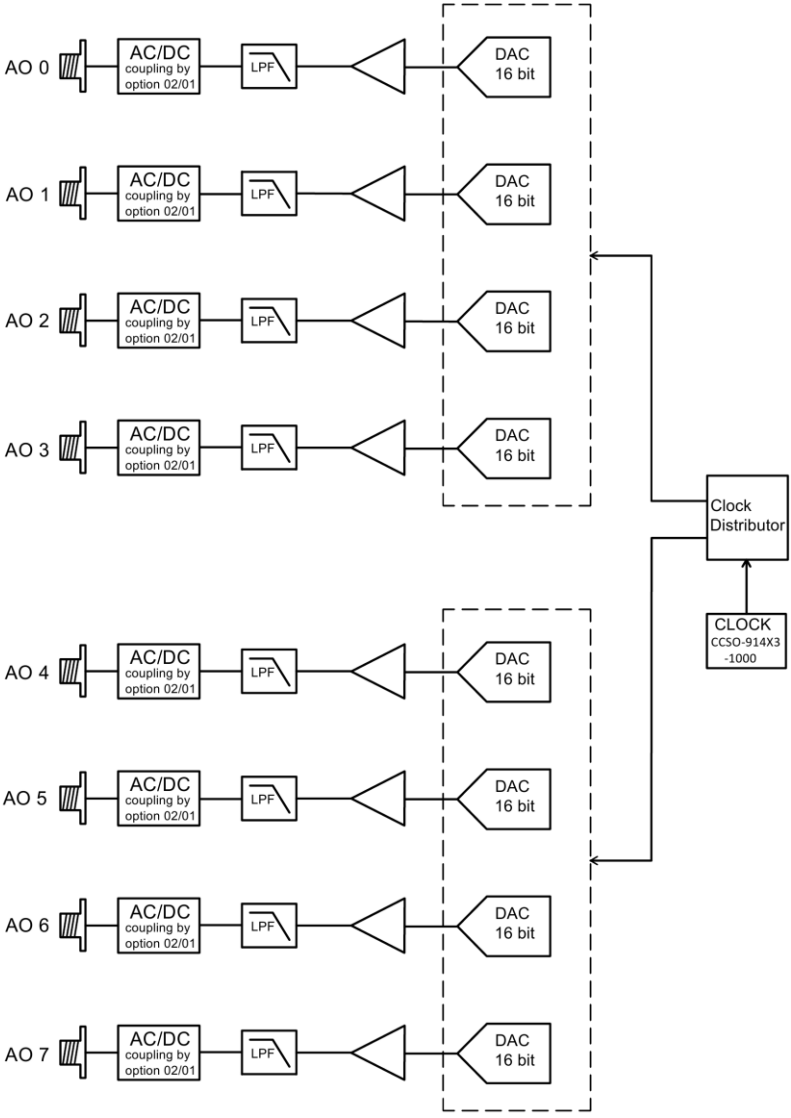
DIO Connector	Pin	Signal	Signal Description
	1	Port 0 (DIO 0)	Bidirectional single-ended (SE) digital I/O (DIO) data channel.
	2	GND	Ground reference for signals.
	3	Port 0 (DIO 1)	Bidirectional SE DIO data channel.
	4	Port 0 (DIO 2)	Bidirectional SE DIO data channel.
	5	GND	Ground reference for signals.
	6	Port 0 (DIO 3)	Bidirectional SE DIO data channel.
	7	Port 1 (DIO 0)	Bidirectional SE DIO data channel.
	8	GND	Ground reference for signals.
	9	Port 1 (DIO 1)	Bidirectional SE DIO data channel.
	10	Port 1 (DIO 2)	Bidirectional SE DIO data channel.
	11	GND	Ground reference for signals.
	12	Port 1 (DIO 3)	Bidirectional SE DIO data channel.
	13	Port 2 (DIO 0)	Bidirectional SE DIO data channel.
	14	+3.3 V	+3.3 V power (50 mA maximum).
	15	Port 2 (DIO 1)	Bidirectional SE DIO data channel.
	16	Port 2 (DIO 2)	Bidirectional SE DIO data channel.
	17	GND	Ground reference for signals.
	18	+3.3 V	+3.3 V power (50 mA maximum).
	19	Port 2 (DIO 3)	Bidirectional SE DIO data channel.

Caution The DIO connector accepts a standard, third-party HDMI cable, but the DIO port is not an HDMI interface. Do not connect the DIO port on the MT1105 to the HDMI port of another device. MT is not liable for any damage resulting from such signal connections.

Block Diagram

The following figure shows the MT1105 block diagram.

Figure 3. MT1105 Block Diagram



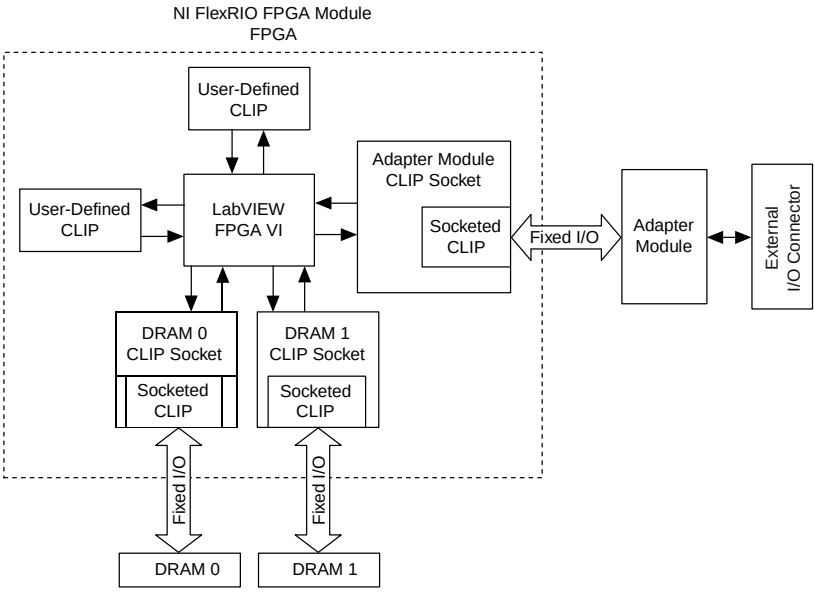
MT1105 Component-Level Intellectual Property (CLIP)

The LabVIEW FPGA Module includes component-level intellectual property (CLIP) for HDL IP integration.NI FlexRIO devices support two types of CLIP: user-defined and socketed.

- *User-defined CLIP* allows you to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- *Socketed CLIP* provides the same IP integration of the user-defined CLIP, but also allows the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

The following figure shows the relationship between an FPGA VI and the CLIP.

Figure 4.CLIP and FPGA VI Relationship



The MT1105 ships with socketed CLIP items that add module I/O to the LabVIEW project.

MT1105 CLIP

The MT1105 CLIP provides access to two receive channels and four transmit channels. The CLIP also provides a User Command interface for common configurations of the baseband clocking.

Configure the baseband clocking using one of the following settings:

- Internal Sample Clock
- Internal Sample Clock locked to an external Reference Clock though the CLK IN connector
- External Sample Clock through the CLK IN connector
- Internal Sample Clock locked to an external Reference Clock through the Sync Clock

This CLIP also contains a SPI interface, which directly programs registers on all programmable devices, such as the digital-to-analog converter (DAC). Programming registers on these devices allows for more advanced configuration.

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Programmable Chips

You can program the following chips from the CLIP.

Table 4. Programmable Chips

Chip
DAC
Clock Oscillator1 GHz

Using Your MT1105with a LabVIEW FPGA Example VI

Note You must install the software before running this example. Refer to the *NI FlexRIO FPGA Installation Guide and Specifications* for more information about installing your software.

The NI FlexRIO Adapter Module Support software includes an example project to help you get started creating your LabVIEW FPGA application. This section explains how to use an existing LabVIEW FPGA example project to generate and acquire samples with the MT1105. This example requires at least one SMA cable for connecting signals to your MT1105.

Note The examples available for your device are dependent on the version of the software and driver you are using. For more information about which software versionsarecompatiblewithyourdevice,visitni.com/info, enter rd software version in the text field, and click the NI FlexRIO link in the results.

The MT1105 example project includes the following components:

- A LabVIEW FPGA VI that can be compiled and run on the FPGA embedded in the hardware
- At least one VI that runs on Windows and interacts with the LabVIEW FPGA VI

Note In the LabVIEW FPGA Module software, NI FlexRIO adapter modules are referred to as *IO Modules.*

Using the Included Streaming Example

Complete the following steps to run an example that generating a wave form using the MT1105.

1. Connect an scope to the AO 0 connector on the front panel of the MT1105.
2. Launch LabVIEW.
3. Select **File**» **Open Project**.
4. Navigateto`<labview>\examples\instr\MT1105\Getting Started`.
5. Select **MT1105 Getting Started. lvproj**.
6. In the **Project Explorer** window, select **MT1105 Getting Started (Host).vi** under **My Computer** to open the host VI. The Open FPGA VI Reference function in this VI uses the NI 7965R as the FPGA target by default. If you are using an NI FlexRIO FPGA module other than the NI 7965R, complete the following steps to change to the FPGA VI to support your target.
   a) On the block diagram, right-click the Open FPGA VI Reference (PXI-7965R) function and select **Configure Open FPGA VI Reference**.
   b) In the **Configure Open FPGA VI Reference** dialog box, click the **Browse** button next to the **Bitfile** button.
   c) In the **Select Bitfile** dialog box that opens, select the bitfile for your desired target. The bitfile name is based on the adapter module, example type, and FPGA module.
   d) Click the **Select** button.
   e) Click **OK** in the **Configure Open FPGA VI Reference** dialog box.
   f) Save the VI.
7. On the front panel, in the **RIO Device** pull-down menu, select an MT1105resource that corresponds with the target configured in step 6.
8. Click the **Run** button to run the VI.
9. The VI acquires data and displays the captured waveform on the **Timing Diagram and Power Spectrum** graphs.
10. Click the **STOP** button to stop the VI.
11. Close the VI.

Creating a LabVIEW Project

This section explains how to set up your target and create an FPGA VI and host VI for data communication. This section focuses on proper project configuration, proper CLIP configuration, and how to access MT1105 I/O nodes.

Creating a Project

1. Launch LabVIEW, or if LabVIEW is already running, select **File**» **Create Project**.
2. In the **Create Project** dialog box, select **LabVIEW FPGA Project** and click **Finish**.
3. Select **FlexRIO on My Computer** and click **Next**.

4. Either discover a LabVIEW FPGA target in your system or create a new system and specify an FPGA target for which to construct a project.
5. Click **Finish** in the **Project Preview** dialog box.
6. Click **File**» **Save** and specify a name for the project.

Creating an FPGA Target VI

1. In the **Project Explorer** window, expand **FPGA Target**.
2. Right-click **IO Module** in the **Project Explorer** window and select **Properties**.
3. Select **Enable IO Module**.
4. Select the MT1105from the **IO Module** list. The available CLIP for the MT1105is displayed in the **Component Level IP** pane.
5. Select MT1105 in the **Name** list of the **Component Level IP** pane.
6. Right-click **FPGA Target** and select **New**» **FPGA Base Clock**.
7. In the **Resource** pull-down menu, select **IO Module Clock 0**and click **OK**.
8. Right-click **FPGA Target** and select **New**» **FPGA Base Clock**.
9. In the **Resource** pull-down menu, select **IO Module Clock 1** and click **OK**.

Note Configuring these clocks is required for proper CLIP operation. Refer to the MT1105 CLIP topics in the *NI FlexRIO Help* for more information about configuring your clocks.

10. Select **File**» **Open** and select `<labview>\examples\instr\MT1105\Getting Started\MT1105 FPGA.vi`.
11. Select **File**» **Save As**.
12. Select **Copy**» **Open Additional Copy** and check **Add Copy to <your project name>.lvproj**.
13. Select the destination folder for the new file, specify a file name, and click **OK**. Use this FPGA VI with the MT1105 Configuration Design Library.
14. Add any FPGA code, controls, and indicators that you need. Refer to `MT1105 Getting Started. lvproj` for example FPGA code, controls, and indicators.
15. Click the **Run** button. LabVIEW creates a default build specification and begins compiling the VI. The **Generating Intermediate Files** window displays the code generation process. The **Compilation Status** window displays the progress of the compilation. The compilation takes several minutes.
16. Click **Close** in the **Compilation Status** window.
17. Save and close the VI.
18. Save the project.

Creating a Host VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New**» **VI** to open a blank VI.
2. Select **Window**» **Show Block Diagram** to open the VI block diagram.
3. Add the Open FPGA VI Reference function from the FPGA Interface palette to the block diagram.
4. Right-click the Open FPGA VI Reference function and select **Configure Open FPGA VI Reference**.
5. In the **Configure Open FPGA VI Reference** dialog box, select **VI** in the **Open** section.
6. In the **Select VI** dialog box, select your project under your device and click **OK**.
7. Click **OK** in the **Configure Open FPGA VI Reference** dialog box. The target name appears under the Open FPGA VI Reference function in the block diagram.
8. Select **File**» **Open** and select `<labview>\instr.lib\MT1105\`
9. Add any VIs from this folder that you need.
10. Open the FPGA Interface palette.
11. Add any Read/Write Control or Invoke Method nodes necessary to configure and communicate with your FPGA VI.
12. Add the Close FPGA VI Reference function to your block diagram.
13. Wire the FPGA VI Reference function to the Close FPGA VI Reference function.
14. Save and close the VI.
15. Save the project.

Run the Host VI

1. Open the front panel of your host VI.
2. Click the **Run** button to run the VI.

MT1105 Configuration Design Library

The MT1105 Configuration Design Library consists of host and FPGA VIs that provide an interface to configure the hardware on the MT1105.

The library allows you to perform the following actions:

- Configure the RF signal path
- Read from and write to the EEPROM
- Configure the clocks
- Reinitialize the CLIP
- Query for CLIP errors

The MT1105 Configuration Design Library relies on the Register Bus Design Library. The Register Bus provides a packet-based configuration interface which exposes all of the address spaces of the configurable chips and subsystems of the adapter module, without requiring hundreds of controls and indicators on your FPGA VI front panel.

The MT1105 Configuration Design Library host VIs all require a register bus object for the device you want to configure. Create the register bus object using Open Session.vi, or use MT1105 Open.vi.

FPGA VI Requirements

Copy all the controls, indicators, and FPGA logic required to use the MT1105 Configuration Design Library from the following VI:`<labview>\instr.lib\MT1105\MT1105 Open.vi`.The FAM Support installer installs this VI on your system.

Configure your FPGA target to contain a FIFOs with the following configuration.

- Names: `DAC CH0 FIFO /DAC CH1 FIFO -/- DAC CH7 FIFO`
- Type: Host to Target - DMA
- Requested number of elements: 16384
- Data type: U16
- Arbitration for read: Arbitrate if multiple requestors only
- Number of elements per read: 1

Configure your FPGA target to contain a memories with the following configuration.

- Names: `DAC Memory – CH0 /DAC Memory – CH1 -/- DAC Memory – CH7`
- Requested number of elements: 16384
- Data type: U16
- Interface A Arbitration: Arbitrate if multiple requestors only
- Interface B Method: Write
- Interface B Arbitration: Arbitrate if multiple requestors only

Host VI Requirements

Configure your host VI to use the MT1105 Configuration Design Library using the following configuration:

1. Create a Register Bus object for your device and initialize the session using MT1105 Open.vi.
2. Use any of the MT1105 Configuration Design Library Host VIs using the Register Bus object returned by the MT1105 Open VI.
3. To access the Host VIs, select **Functions**» **Instrument I/O**» **Instrument Drivers**» **MT1105**.
4. Close the session using the MT1105 Close VI.

Clocking

The MT1105 clock source controls the sample rate and other timing functions on the device. The following table contains information about the possible MT1105 clock sources.

Table 5. MT1105 Clock Sources

Clock	Frequency	Source Options
Sample Clock	250 MHz	• Free-running and internally sourced
Reference Clock	250 MHz	• External through the CLK IN front panel connector

Type of Clock Oscillator - CCSO-914X3-1000 (1 GHz):

Phase Noise Typical:	1kHz	-112 dBc/Hz
	10kHz	-142 dBc/Hz
	100kHz	-155 dBc/Hz
	1MHz	-167 dBc/Hz
	10MHz	-168 dBc/Hz

MT1105 Specifications

Specifications are warranted by design and under the following conditions unless otherwise noted:

- Chassis fan speed is set to High. In addition, NI recommends using slot blockers and EMC filler panels in empty module slots to minimize temperature drift.
- The MT1105 uses NI LabVIEW and LabVIEW FPGA software.

Specifications describe the warranted product performance over ambient temperature ranges of 0 °C to 55 °C, unless otherwise noted.

Typical values describe useful product performance beyond specifications that are not covered by warranty and do not include guard bands for measurement uncertainty or drift. Typical values may not be verified on all units shipped from the factory. Unless otherwise noted, typical values cover the expected performance of units over ambient temperature ranges of 23 °C ± 5 °C with a 90% confidence level, based on measurements taken during development or production.

Nominal values (or supplemental information) describe additional information about the product that may be useful, including expected performance that is not covered under *Specifications* or *Typical* values. Nominal values are not covered by warranty.

Related Information

Front Panel and Connector Pinouts on page6
Connecting Cables on page 4
MT1105User Manual and Specifications on page 1

AO 0÷7 Front Panel Connectors

Amplitude Range

AO output range ..... 1.4V (pp)

Typical Characteristics

Note All values are typical.

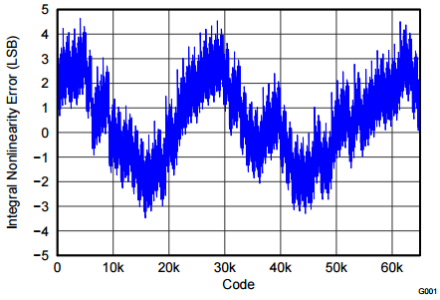


Figure 15. Integral Nonlinearity

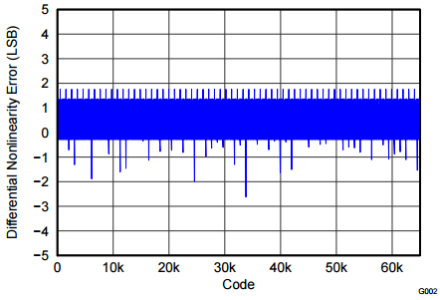


Figure 16. Differential Nonlinearity

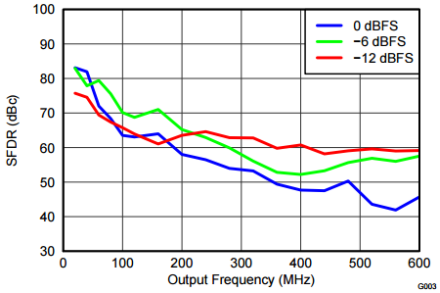


Figure 17. SFDR vs Output Frequency Over Input Scale

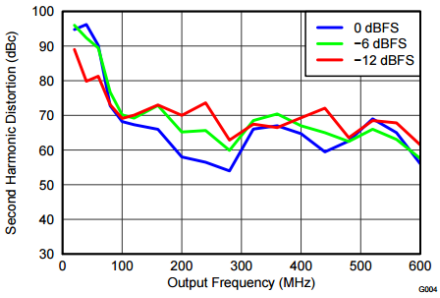


Figure 18. Second Harmonic Distortion vs Output Frequency Over Input Scale

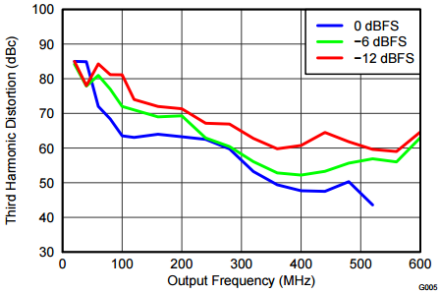


Figure 19. Third Harmonic Distortion vs Output Frequency Over Input Scale

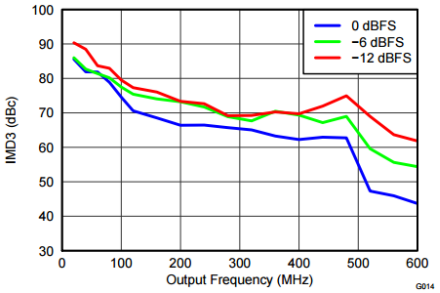


Figure 19.IMD3 vs Output Frequency Over Input Scale

CLK IN Front Panel Connector

Frequency

Sample Clock.....250 MHz

Amplitude

Square.....0.7$V_{pk-pk}$to 5.0V_{pk-pk} into 50Ω, typical

Sine.....1.4$V_{pk-pk}$to 5.0V_{pk-pk} (1$V_{RMS}$to 3.5V_{RMS}) into 50Ω, typical

Input impedance.....50Ω, nominal

Coupling.....AC

Baseband Characteristics

DAC

Resolution.....16 bits

Data rate.....250 MS/s (automatically interpolated to 1GS/s)

Samples per cycle.....1

Dimensions and Weight

Dimensions.....12.9 × 2.0 × 12.1 cm (5.1 × 0.8 × 4.7 in)

Weight.....413 g (14.6 oz)

I/O.....AO 0, AO1, AO 2, AO 3, AO 4, AO 5, AO 6, AO 7, CLK IN

Power.....3 W, nominal

DIO (DIO <0...11>, and+3.3 V power)

General Characteristics

Number of channels.....12 bidirectional (12 DIO and 2 Pw)

Connector type.....HDMI

Interface standard.....3.3 LVCMOS

Interface logic

- Maximum V_{IL}.....0.8V
- Minimum V_{IH}.....2.0V
- Maximum V_{OL}.....0.4V
- Minimum V_{OH}.....2.7V
- Maximum V_{OH}.....3.6V
- Z_{OUT}.....50Ω±20%
- I_{OUT}(DC).....±2mA

Pull-down resistor.....150 kΩ

Recommended operating voltage.....-0.3 V to 3.6 V Overvoltage

Protection .....±5 V

Maximum toggle frequency.....6,6 MHz

+3.3 V maximum power.....100 mA

+3.3 V voltage tolerance.....3.1 V to 3.4 V

Operating Environment

Ambient temperature range.....0 °C to 55 °C

Relative humidity range.....10% to 90%,

Storage Environment

Ambient temperature range.....-40 °C to 70 °

Relative humidity range.....5% to 95%

Operational shock.....30 g peak, half-sine, 11 ms pulse

Random vibration

Operating .....5Hz to 500Hz, 0.3 g_{rms}

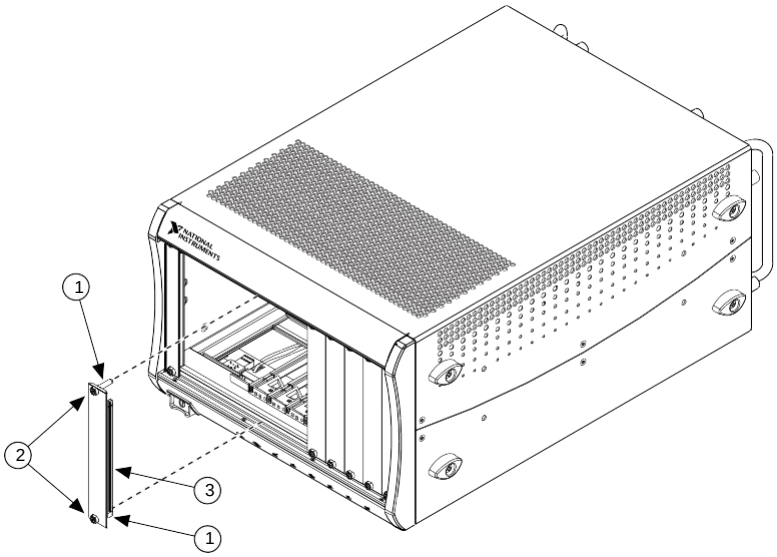
Non operating .....5Hz to 500 Hz, 2.4g_{rms}

Installing PXI EMC Filler Panels

To ensure specified EMC performance, PXI EMC filler panels must be properly installed in your FlexRIO system. The PXI EMC filler panels (National Instruments part number 778700-01) must be purchased separately. For more installation information, refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications*.

1. Remove the captive screw covers.
2. Install the PXI EMC filler panels by securing the captive mounting screws to the chassis, as shown in the figure below. Make sure that the EMC gasket is on the right side of the PXI EMC filler panel.

Figure 13.PXI EMC Filler Panels and Chassis



1. Captive Screw Covers
2. Captive Mounting Screws
3. EMC Gasket

Note You must populate all slots with a module or a PXI EMC filler panel to ensure proper module cooling. Do not over tighten screws (2.5 lb · in maximum). For additional information about the use of PXI EMC filler panels in your PXI system, visit `ni.com/info` and enter `emc panels`.

Related Information

Electromagnetic Compatibility Guidelines on page 3

Where to Go for Support

The Mush Technologies Web site is your complete resource for technical support. At www.mush-tech.com you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from MT Application Engineers.

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