USER MANUAL AND SPECIFICATIONS

MT1115

2-Channel Signal Generator Adapter Module

The MT1115 is a two-channel, 1.25 GS/s, 16-bit, 600 MHz Analog Bandwidth (with no compensation for DAC sinc response) , High-Speed Signal Generator adapter module designed to work in conjunction with your NI FlexRIO™ FPGA module.

The 2-Channel Signal Generator Adapter Module designed to work in conjunction with your NI FlexRIO™ FPGA module. The MT1115 features the following connectors and chips:

- 2-channel, 1.25 GS/s digital-to-analog converter (DAC) with 16-bit accuracy
- Timing chip with clocking options from the backplane and the front panel
- The following front panel connectors:
  - TRIG IN
  - CLK IN
  - AO 0+
  - AO 0-
  - AO 1+
  - AO 1-
  - DIO

This document contains signal information and lists the specifications of the MT1115, which is composed of the NI Flex RIO FPGA module and the MT1115. This document also contains tutorial sections that demonstrate how to acquire data using a LabVIEW FPGA Example VI and how to create and run your own LabVIEW project with the MT1115.

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Note MT1115 refers to the combination of your MT1115 adapter module and your NI FlexRIO FPGA module. MT1115 refers to your MT1115 adapter module only.

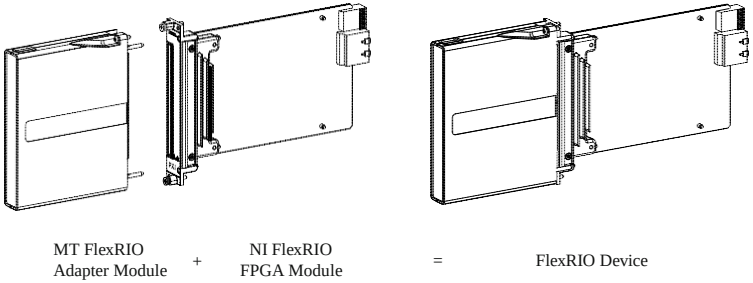
Note The MT1115 is only compatible with the NI PXIe-796xR FPGA modules.

Note Before configuring your MT1115, you must install the appropriate software and hardware. Refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications* for installation instructions.

Note For EMC compliance, operate this device according to the documentation.

The following figure shows an example of a properly connected FlexRIO device.

Figure 1. FlexRIO Device



Related Information

MT1115 Specifications on page 17

Contents

Electromagnetic Compatibility Guidelines

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC) stated in the product specifications. These requirements and limits are designed to provide reasonable protection against harmful interference when the product is operated in the intended operational electromagnetic environment.

This product is intended for use in industrial locations. However, harmful interference may occur in some installations, when the product is connected to a peripheral device or test object, or if the product is used in residential or commercial areas. To minimize interference with radio and television reception and prevent unacceptable performance degradation, install and use this product in strict accordance with the instructions in the product documentation.

Furthermore, any modifications to the product not expressly approved by Mush Technologies could void your authority to operate it under your local regulatory rules.

Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

Caution To ensure the specified EMC performance, the length of all I/O cables must be no longer than 3 m (10 ft).

Caution To ensure the specified EMC performance, you must install PXI EMC Filler Panels (National Instruments part number 778700-1) in adjacent chassis slots.

Connecting Cables

1. Use any shielded 50 Ω SMB cable to connect signals to the connectors on the front panel of your device.

How to Use Your NI FlexRIO Documentation Set

Refer to Figure 2 and Table 1 to learn how to use your FlexRIO documentation set.

Figure 2. How to Use Your NI FlexRIO Documentation Set.

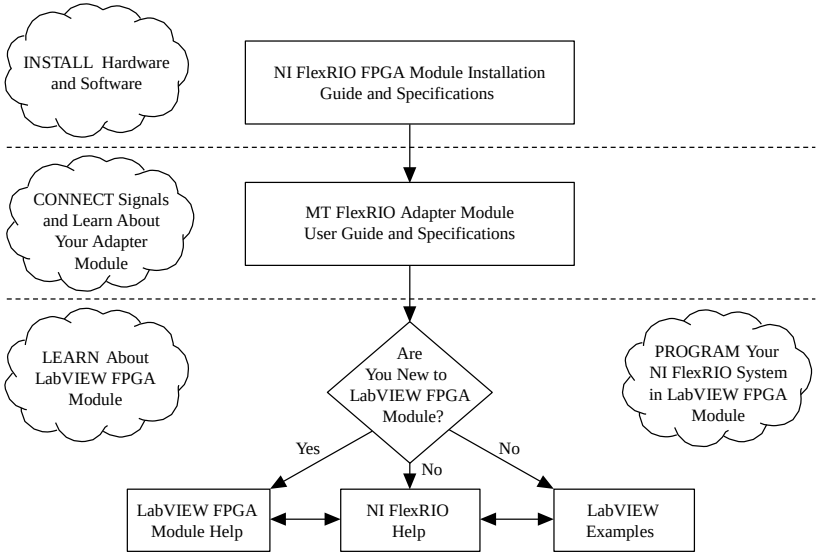


Table 1. NI FlexRIO Documentation Locations and Descriptions

Document	Location	Description
NI FlexRIO FPGA Module Installation Guide and Specifications	Available from the Start menu and at ni.com/manuals.	Contains installation instructions for your NI FlexRIO system and specifications for your FPGA module.
MT1115 User Manual and Specifications (this document)	Available from at www.mush-tech.com/	Contains signal information, examples, CLIP details, and specifications for your adapter module.
LabVIEW FPGA Module Help	Embedded in *LabVIEW Help* and at ni.com/manuals.	Contains information about the basic functionality of the LabVIEW FPGA Module.
NI FlexRIO Help	Available from the Start menu and at ni.com/manuals.	Contains FPGA Module, adapter module, and CLIP configuration information.
LabVIEW Examples	Available in NI Example Finder.	Contains examples of how to run FPGA VIs and Host VIs on your device.

Table 1. NI FlexRIO Documentation Locations and Descriptions (Continued)

Document	Location	Description
IP Net	ni.com/ipnet	Contains LabVIEW FPGA functions and intellectual property to share.
NI FlexRIO product page	ni.com/flexrio	Contains product information and data sheets for NI FlexRIO devices.

Key Features

The MT1115 includes the following key features:

Instantaneous bandwidth .....600 MHz

DAC .....16-bit channel at 1.25 GS/s
(DC coupled Option- 01); (AC coupled Option- 02)

Configuration

You can configure the MT1115 as follows:

- Instantaneous bandwidth up to 600 MHz
- 2 differential transmitter channel, 16-bit, 1.25 GS/s

Front Panel and Connector Pinouts

Table 2 shows the front panel connector and signal descriptions for the MT1115.

Caution To avoid permanent damage to the MT1115, disconnect all signals connected to the MT1115 before powering down the module, and connect signals only after the adapter module has been powered on by the NI FlexRIO FPGA module

Caution Connections that exceed any of the maximum ratings of any connector on the MT1115 can damage the device and the chassis. NI is not liable for any damage resulting from such connections.

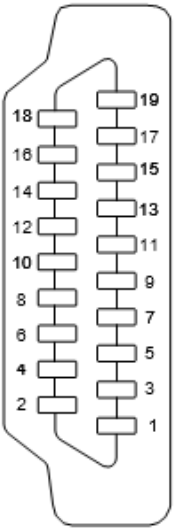
Related Information
MT1115 Specifications on page 17

Table 2. Front panel connector and signal descriptions for the MT1115

Device Front Panel	Connector	Signal Description
	TRIG IN	Input connector for Trigger IN, 50 Ω single-ended, +20 dBm max.
	CLK IN	Reference Clock input, 50 Ω single-ended, +20 dBm maximum
	AO 0+	Analog Output Channel 0+, differential analog output channel
	AO 0-	Analog Output Channel 0- , differential analog output channel
	AO 1+	Analog Output Channel 1+, differential analog output channel
	AO 1-	Analog Output Channel 1- , differential analog output channel
	DIO	Refer to Table 3 for the signal list and descriptions.

DIO Connector

Table 3. MT1115 DIO Connector Pin Assignments

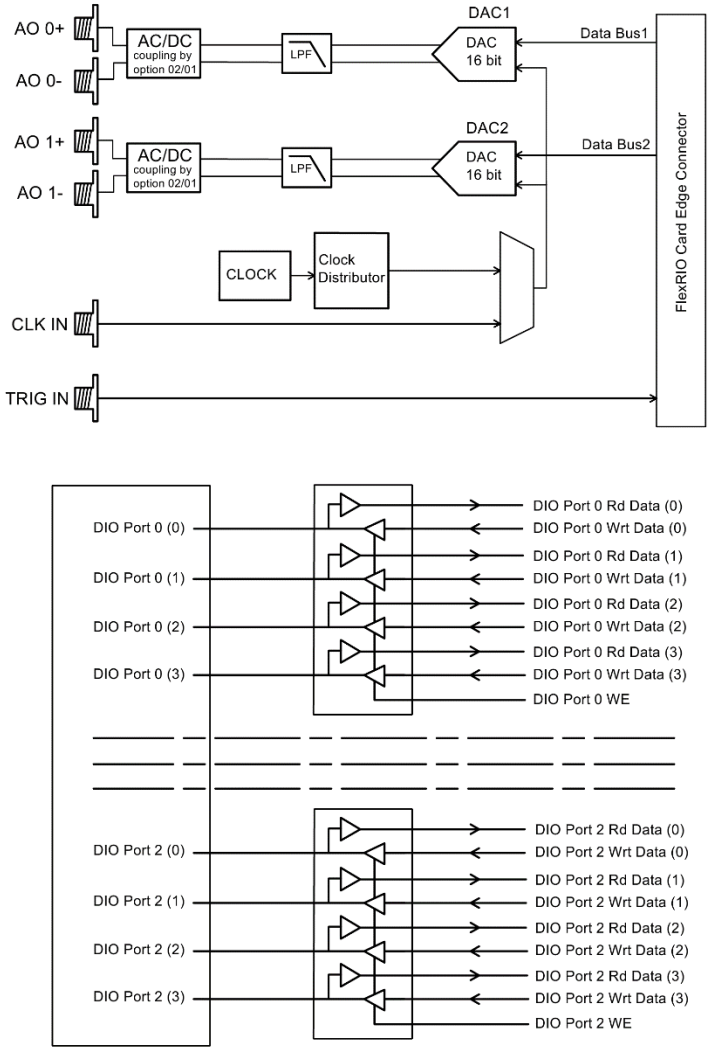
DIO Connector	Pin	Signal	Signal Description
	1	Port 0 (DIO 0)	Bidirectional single-ended (SE) digital I/O (DIO) data channel.
	2	GND	Ground reference for signals.
	3	Port 0 (DIO 1)	Bidirectional SE DIO data channel.
	4	Port 0 (DIO 2)	Bidirectional SE DIO data channel.
	5	GND	Ground reference for signals.
	6	Port 0 (DIO 3)	Bidirectional SE DIO data channel.
	7	Port 1 (DIO 0)	Bidirectional SE DIO data channel.
	8	GND	Ground reference for signals.
	9	Port 1 (DIO 1)	Bidirectional SE DIO data channel.
	10	Port 1 (DIO 2)	Bidirectional SE DIO data channel.
	11	GND	Ground reference for signals.
	12	Port 1 (DIO 3)	Bidirectional SE DIO data channel.
	13	Port 2 (DIO 0)	Bidirectional SE DIO data channel.
	14	+3.3 V	+3.3 V power (50 mA maximum).
	15	Port 2 (DIO 1)	Bidirectional SE DIO data channel.
	16	Port 2 (DIO 2)	Bidirectional SE DIO data channel.
	17	GND	Ground reference for signals.
	18	+3.3 V	+3.3 V power (50 mA maximum).
	19	Port 2 (DIO 3)	Bidirectional SE DIO data channel.

Caution The AUX I/O connector accepts a standard, third-party HDMI cable, but the AUX I/O port is not an HDMI interface. Do not connect the AUX I/O port on the MT1115 to the HDMI port of another device. MT is not liable for any damage resulting from such signal connections.

Block Diagram

The following figure shows the MT1115 block diagram.

Figure 3. MT1115 Block Diagram



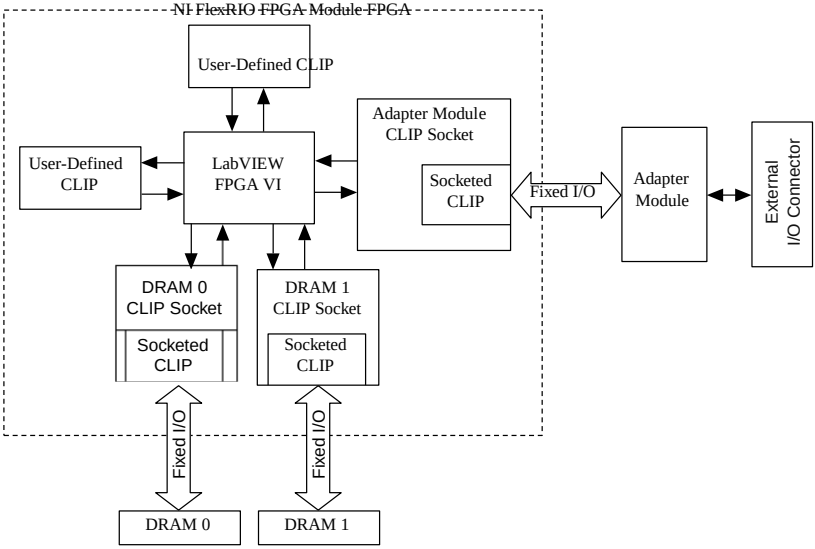
MT1115 Component-Level Intellectual Property (CLIP)

The LabVIEW FPGA Module includes component-level intellectual property (CLIP) for HDL IP integration. NI FlexRIO devices support two types of CLIP: user-defined and socketed.

- *User-defined CLIP* allows you to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- *Socketed CLIP* provides the same IP integration of the user-defined CLIP, but also allows the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

The following figure shows the relationship between an FPGA VI and the CLIP.

Figure 4. CLIP and FPGA VI Relationship



The MT1115 ships with socketed CLIP items that add module I/O to the LabVIEW project.

The MT1115 CLIP provides access to two transmit channels. The CLIP also provides a User Command interface for common configurations of the baseband clocking.

Configure the baseband clocking using one of the following settings:

- Internal Sample Clock
- Internal Sample Clock locked to an external Reference Clock though the CLK IN connector
- External Sample Clock through the CLK IN connector
- Internal Sample Clock locked to an external Reference Clock through the Sync Clock

This CLIP also contains a SPI interface, which directly programs registers on all programmable devices, such as the digital-to-analog converter (DAC). Programming registers on these devices allows for more advanced configuration.

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Using Your MT1115 with a LabVIEW FPGA Example VI

Note You must install the software before running this example. Refer to the *NI FlexRIO FPGA Installation Guide and Specifications* for more information about installing your software.

The NI FlexRIO Adapter Module Support software includes an example project to help you get started creating your LabVIEW FPGA application. This section explains how to use an existing LabVIEW FPGA example project to generate and acquire samples with the MT1115. This example requires at least one SMA cable for connecting signals to your MT1115.

Note The examples available for your device are dependent on the version of the software and driver you are using. For more information about which software versions are compatible with your device, visit ni.com/info, enter rdsoftwareversionin the text field, and click the NI FlexRIO link in the results.

The MT1115 example project includes the following components:

- A LabVIEW FPGA VI that can be compiled and run on the FPGA embedded in the hardware
- At least one VI that runs on Windows and interacts with the LabVIEW FPGA VI

Note In the LabVIEW FPGA Module software, NI FlexRIO adapter modules are referred to as *IO Modules*.

Using the Included Streaming Example

Complete the following steps to run an example that acquires a waveform using the MT1115.

1. Connect a scope to the AO 0+ connector on the front panel of the MT1115.
2. Launch LabVIEW.
3. Select **File»Open Project**.
4. Navigate to <labview>\examples\instore\MT1115\Getting Started.
5. Select **MT1115 Getting Started.lvproj**.
6. In the **Project Explorer** window, select **MT1115 Getting Started (Host).vi** under **My Computer** to open the host VI. The Open FPGA VI Reference function in this VI uses the NI 7965R as the FPGA target by default. If you are using an NI FlexRIO FPGA module other than the NI 7965R, complete the following steps to change to the FPGA VI to support your target.
    a) On the block diagram, right-click the Open FPGA VI Reference (PXI-7965R) function and select **Configure Open FPGA VI Reference**.
    b) In the **Configure Open FPGA VI Reference** dialog box, click the **Browse** button next to the **Bitfile** button.
    c) In the **Select Bitfile** dialog box that opens, select the bitfile for your desired target. The bitfile name is based on the adapter module, example type, and FPGA module.
    d) Click the **Select** button.
    e) Click **OK** in the **Configure Open FPGA VI Reference** dialog box.
    f) Save the VI.
7. On the front panel, in the **RIO Device** pull-down menu, select an MT1115 resource that corresponds with the target configured in step 6.
8. Click the **Run** button to run the VI.
9. The VI acquires data and displays the captured waveform on the **Timing Diagram and Power Spectrum** graphs.
10. Click the **STOP** button to stop the VI.
11. Close the VI.

Creating a LabVIEW Project

This section explains how to set up your target and create an FPGA VI and host VI for data communication. This section focuses on proper project configuration, proper CLIP configuration, and how to access MT1115 I/O nodes.

Creating a Project

1. Launch LabVIEW, or if LabVIEW is already running, select **File»Create Project**.
2. In the **Create Project** dialog box, select **LabVIEW FPGA Project** and click **Finish**.
3. Select **FlexRIO on My Computer** and click **Next**.

4. Either discover a LabVIEW FPGA target in your system or create a new system and specify an FPGA target for which to construct a project.
5. Click **Finish** in the **Project Preview** dialog box.
6. Click **File**»**Save** and specify a name for the project.

Creating an FPGA Target VI

1. In the **Project Explorer** window, expand **FPGA Target**.
2. Right-click **IO Module** in the **Project Explorer** window and select **Properties**.
3. Select **Enable IO Module**.
4. Select the MT1115 from the **IO Module** list. The available CLIP for the MT1115 is displayed in the **Component Level IP** pane.
5. Select MT1115 in the **Name** list of the **Component Level IP** pane.
6. Right-click **FPGA Target** and select **New**»**FPGA Base Clock**.
7. In the **Resource** pull-down menu, select **IO Module Clock 0** and click **OK**.
8. Right-click **FPGA Target** and select **New**»**FPGA Base Clock**.
9. In the **Resource** pull-down menu, select **IO Module Clock 1** and click **OK**.

Note Configuring these clocks is required for proper CLIP operation. Refer to the MT1115 CLIP topics in the *NI FlexRIO Help* for more information about configuring your clocks.

10. Select **File**»**Open** and select <labview>\examples\instr\MT1115\Getting Started\MT1115 FPGA.vi.
11. Select **File**»**Save As**.
12. Select **Copy**»**Open Additional Copy** and check **Add Copy to <your project name>.lvproj**.
13. Select the destination folder for the new file, specify a file name, and click **OK**. Use this FPGA VI with the MT1115 Configuration Design Library.
14. Add any FPGA code, controls, and indicators that you need. Refer to MT1115 Getting Started.lvprojfor example FPGA code, controls, and indicators.
15. Click the **Run** button. LabVIEW creates a default build specification and begins compiling the VI. The **Generating Intermediate Files** window displays the code generation process. The **Compilation Status** window displays the progress of the compilation. The compilation takes several minutes.
16. Click **Close** in the **Compilation Status** window.
17. Save and close the VI.
18. Save the project.

Creating a Host VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New**»**VI** to open a blank VI.
2. Select **Window**»**Show Block Diagram** to open the VI block diagram.
3. Add the Open FPGA VI Reference function from the FPGA Interface palette to the block diagram.
4. Right-click the Open FPGA VI Reference function and select **Configure Open FPGA VI Reference**.
5. In the **Configure Open FPGA VI Reference** dialog box, select **VI** in the **Open** section.
6. In the **Select VI** dialog box, select your project under your device and click **OK**.
7. Click **OK** in the **Configure Open FPGA VI Reference** dialog box. The target name appears under the Open FPGA VI Reference function in the block diagram.
8. Select **File**»**Open** and select <labview>\instr.lib\MT1115\
9. Add any VIs from this folder that you need.
10. Open the FPGA Interface palette.
11. Add any Read/Write Control or Invoke Method nodes necessary to configure and communicate with your FPGA VI.
12. Add the Close FPGA VI Reference function to your block diagram.
13. Wire the FPGA VI Reference function to the Close FPGA VI Reference function.
14. Save and close the VI.
15. Save the project.

Run the Host VI

1. Open the front panel of your host VI.
2. Click the **Run** button to run the VI.

MT1115 Configuration Design Library

The MT1115 Configuration Design Library consists of host and FPGA VIs that provide an interface to configure the hardware on the MT1115.

The library allows you to perform the following actions:

- Configure the RF signal path
- Read from and write to the EEPROM
- Configure the clocks
- Reinitialize the CLIP
- Query for CLIP errors

The MT1115 Configuration Design Library relies on the Register Bus Design Library. The Register Bus provides a packet-based configuration interface which exposes all of the address spaces of the configurable chips and subsystems of the adapter module, without requiring hundreds of controls and indicators on your FPGA VI front panel.

The MT1115 Configuration Design Library host VIs all require a register bus object for the device you want to configure.

FPGA VI Requirements

Copy all the controls, indicators, and FPGA logic required to use the MT1115 Configuration Design Library from the following VI: <labview>\instr.lib\MT1115\MT1115 Open .vi. The FAM Support installer installs this VI on your system.

Configure your FPGA target to contain a memories with the following configuration.

- Names: DAC Memory - CH0 / DAC Memory – CH1 / DAC Memory – CH2 / DAC Memory – CH3
- Requested number of elements: 65536
- Data type: U16
- Interface A Arbitration: Arbitrate if multiple requestors only
- Interface B Method: Write
- Interface B Arbitration: Arbitrate if multiple requestors only

Host VI Requirements

Configure your host VI to use the MT1115 Configuration Design Library using the following configuration:

1. Create a Register Bus object for your device and initialize the session using MT1115 Open.vi.
2. Use any of the MT1115 Configuration Design Library Host VIs using the Register Bus object returned by the MT1115 Open VI.
3. To access the Host VIs, select **Functions**» **Instrument I/O**» **Instrument Drivers**» **MT1115**.
4. Close the session using the MT1115 Close VI.

Clocking

The MT1115 clock source controls the sample rate and other timing functions on the device. The following table contains information about the possible MT1115 clock sources.

Table 5. MT1115 Clock Sources

Clock	Frequency	Source Options
Sample Clock	1.25 GHz	• Free-running and internally sourced
Reference Clock	1.25 GHz	• External through the CLK IN front panel connector

MT1115 Specifications

Specifications are warranted by design and under the following conditions unless otherwise noted:

- Chassis fan speed is set to High. In addition, NI recommends using slot blockers and EMC filler panels in empty module slots to minimize temperature drift.
- The MT1115 uses NI LabVIEW and LabVIEW FPGA software.

Specifications describe the warranted product performance over ambient temperature ranges of 0 °C to 55 °C, unless otherwise noted.

Specifications are subject to change without notice.

Typical values describe useful product performance beyond specifications that are not covered by warranty and do not include guard bands for measurement uncertainty or drift. Typical values may not be verified on all units shipped from the factory. Unless otherwise noted, typical values cover the expected performance of units over ambient temperature ranges of 23 °C ± 5 °C with a 90% confidence level, based on measurements taken during development or production.

Nominal values (or supplemental information) describe additional information about the product that may be useful, including expected performance that is not covered under *Specifications* or *Typical* values. Nominal values are not covered by warranty.

Related Information

Front Panel and Connector Pinouts on page 6
Connecting Cables on page 4
MT1115 User Manual and Specifications on page 1

AO 0-1 Front Panel Connectors

Amplitude Range

AO output range .....2 Vp-p differential or 1 Vp-p single ended, DC coupled

Typical Characteristics

Note All values are typical.

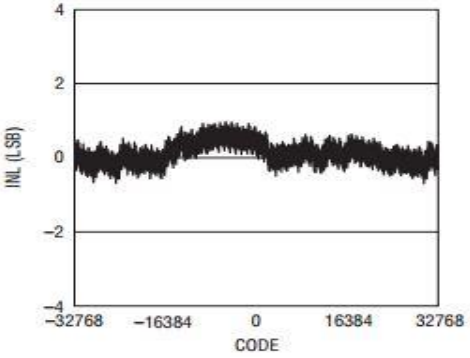

Figure 5. Integral Nonlinearity

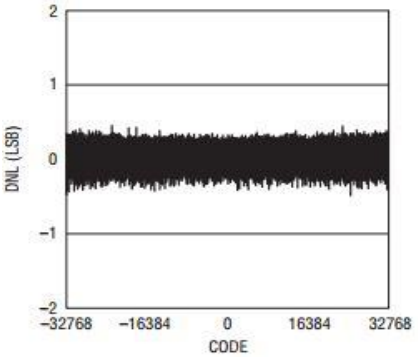

Figure 6. Differential Nonlinearity

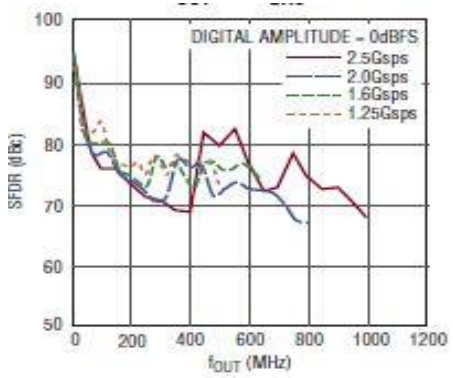

Figure 7. SFDR vs Output Frequency Over Input Scale

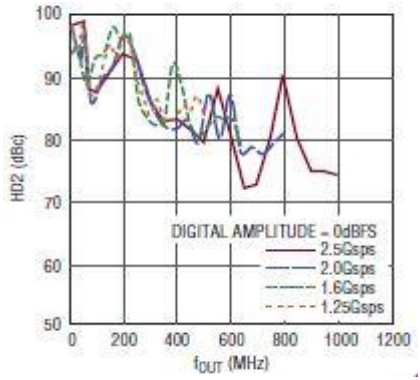

Figure 8. Second Harmonic Distortion vs Output Frequency Over Input Scale

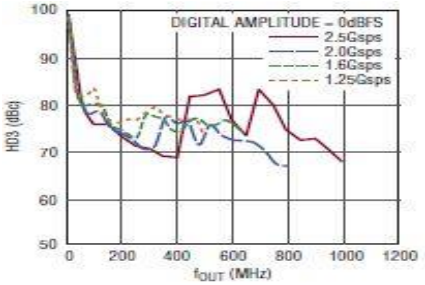

Figure 9. Third Harmonic Distortion vs Output Frequency Over Input Scale

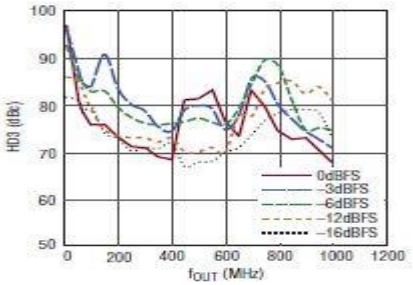

Figure 10. IMD3 vs Output Frequency Over Input Scale

CLK IN Front Panel Connector

Frequency

Reference Clock ..... 1.25 GHz

Sample Clock ..... 1.25 GHz

Amplitude

Square .....0.7 V_{pk-pk} to 5.0 V_{pk-pk} into 50 Ω, typical

Sine .....1.4 V_{pk-pk} to 5.0 V_{pk-pk} (1 V_{RMS} to 3.5 V_{RMS}) into 50 Ω, typical

Input impedance .....50 Ω, nominal

Coupling .....AC

Baseband Characteristics

DAC

Resolution ..... 16 bits

Data rate ..... 1.25 GS/s

Samples per cycle..... 1

Dimensions and Weight

Dimensions .....12.9 × 2.0 × 12.1 cm (5.1 × 0.8 × 4.7 in)

Weight.....413 g (14.6 oz)

I/O .....AO 0+, AO 0-, AO 1+, AO 1-, CLK IN

Power.....3 W, nominal

DIO (DIO <0..11>, and +3.3 V power)

General Characteristics

Number of channels ..... 12 bidirectional (12 DIO and 2 Pw)

Connector type ..... HDMI

Interface standard ..... 3.3 LVCMOS

Interface logic

- Maximum V_{IL} ..... 0.8 V
- Minimum V_{IH} ..... 2.0 V
- Maximum V_{OL} ..... 0.4 V
- Minimum V_{OH} ..... 2.7 V
- Maximum V_{OH} ..... 3.6 V
- Z_{OUT} ..... 50 Ω ± 20%
- I_{OUT} (DC) ..... ±2 mA

Pull-down resistor ..... 150 kΩ

Recommended operating voltage ..... -0.3 V to 3.6 V Overvoltage

protection ..... ±10 V

Maximum toggle frequency ..... 6.6 MHz

+3.3 V maximum current ..... 100 mA

+3.3 V voltage tolerance ..... 3.2 V to 3.4 V

Operating Environment

Ambient temperature range .....0 °C to 55 °

Relative humidity range .....10% to 90%, noncondensing

Storage Environment

Ambient temperature range .....-40 °C to 70 °C

Relative humidity range .....5% to 95%, noncondensing

Operational shock .....30 g peak, half-sine, 11 ms pulse

Random vibration

Operating .....5 Hz to 500 Hz, 0.3 g_{rms}

Nonoperating .....5 Hz to 500 Hz, 2.4

Where to Go for Support

The Mush Technologies Web site is your complete resource for technical support. At http://MUSH-TECH.com/ you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from MT Application Engineers.

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